Fully depleted, thick, monolithic CMOS pixels with high quantum efficiency

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ABSTRACT:

The Centre for Electronic Imaging (CEI) has an active programme of evaluating and designing Complementary Metal-Oxide Semiconductor (CMOS) image sensors with high quantum efficiency, for applications in near-infrared and X-ray photon detection.

This paper describes the performance characterisation of CMOS devices made on a high resistivity 50 μm thick p-type substrate with a particular focus on determining the depletion depth and the quantum efficiency. The test devices contain 8x8 pixel arrays using CCD-style charge collection, which are manufactured in a low voltage CMOS process by ESPROS Photonics Corporation (EPC).

Measurements include determining under which operating conditions the devices become fully depleted. By projecting a spot using a microscope optic and a LED and biasing the devices over a range of voltages, the depletion depth will change, causing the amount of charge collected in the projected spot to change. We determine if the device is fully depleted by measuring the signal collected from the projected spot. The analysis of spot size and shape is still under development.

KEYWORDS: CMOS Image sensor, Characterisation; Depletion Depth.

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Contents

1. Introduction

The Centre for Electronic Imaging (CEI) is expanding its capabilities in Complementary Metal-Oxide Semiconductor (CMOS) image sensor design. Our first test chips have been submitted for manufacture to ESPROS Photonics Corporation (EPC), based in Switzerland. While our first devices are designed and fabricated it is necessary to test and evaluate EPC manufactured devices to determine the operational parameters of their standard processes and explore the technology limitations.

The baseline device characterisation is achieved using the Photon Transfer Curve (PTC) which gives an idea of the overall quality of the device and readout electronics. The PTC is used to produce measurements of linearity, conversion gain, Full Well Capacity (FWC) and read noise **[1]**. Dark current generation is also analysed.

Further work focusses on testing to ensure the device is fully depleted during operation. This is important in a back illuminated sensor to ensure all photo-electrons are captured in the pixel on which they are incident and are not allowed to diffuse laterally in a field free region. A fully depleted back illuminated detector should provide improved Quantum Efficiency (QE) over front illuminated devices.

2. Test Devices

Figure 1 shows one of the test devices provided by EPC for evaluation. The device is an 8x8 array of test pixels consisting of 8 different pixel designs. Referring to the pixel schematic in Figure 2, one half of the 8x8 array is made up of pixels with half-sized storage gates [2]. Unless otherwise stated in the text the measurements presented are taken as an average across the array.

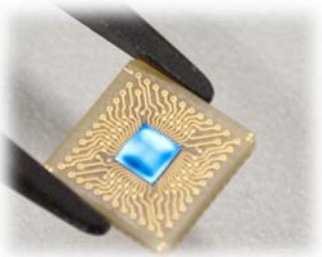

Figure 1: The 8x8 test array mounted on a PCB.

The test pixels used in this study are a backside illuminated dual gate design with an integrated CMOS Active Pixel Sensor (APS) readout, a schematic can be seen in Figure 2. Dual gate refers to a pair of storage gates (SG) which are present in each pixel, however only one such gate is represented in Figure 2 for drawing simplicity. The device substrate is thinned to 50 µm during manufacture, a well-established process for achieving high quantum efficiency in all CCD and CMOS image sensors. The pixel is fully depleted in normal operation due a combination of the use of a high resistivity substrate and the application of a backside bias.

2.1 Pixel Operation

The pixel operates using a series of drift gates (DG) with monotonically increasing bias voltage. When biased, an electro-static field forms along the drift gates and photo-generated charges are directed onto one of the two storage gates, with charge storage controlled by a pair of inversely coupled modulation gates. Each storage gate has a dedicated source follower circuit which buffers the signal to separate outputs (A or B) as shown in Figure 2.

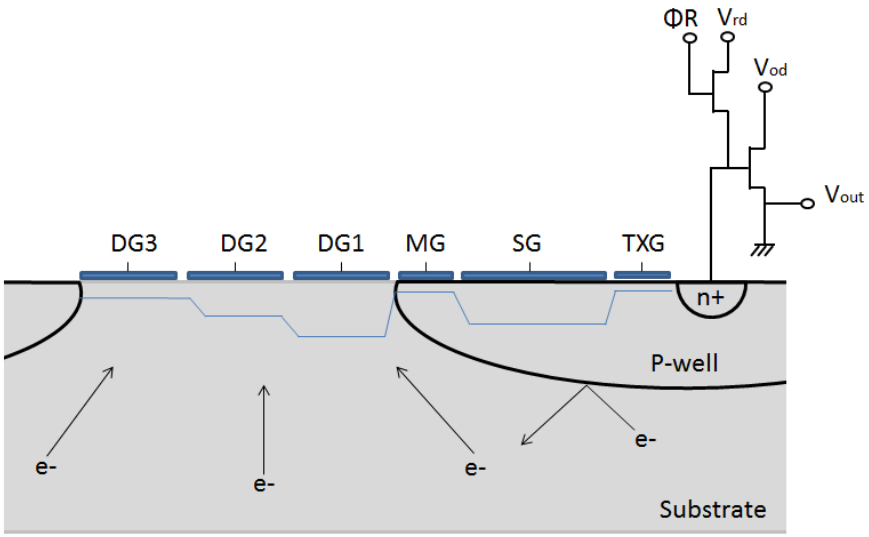

Figure 2: Schematic of the pixel design found in the test devices. This schematic includes only one modulation gate (MG), one storage gate (SG), one transfer gate (TXG) and one output amplifier, in reality there are two of each. ΦR is the reset pulse, Vrd is the reset drain, Vod is the output drain and Vout is the output voltage. Black lines represent doping junctions, while the blue lines give an impression of the potential well profile.

Figure 2 shows that the storage and readout of signal charge is isolated within a p-well which prevents optically generated charges from directly accumulating on the storage gate during integration. Charge is generated in the fully-depleted substrate, and the p-well deflects charge towards the drift gates, so that charge can be stored on the correct storage gate at the correct time – as controlled by the relevant modulation gate.

Test pixels are manufactured on a pitch of 40 µm x 40 µm, this area includes all the gates and the transistors making up the readout buffer, shown in Figure 2.

2.2 Test System

The test devices are driven and read out using the Universal Evaluation System, UES, shown in Figure 3. The universal evaluation system is also produced by EPC and designed so that it is compatible with any EPC manufactured devices, giving the advantage of using the same drive electronics for all devices. The UES is an FPGA based test station which allows automated testing and characterisation of imaging devices manufactured with a standardised pin layout used by EPC **[3].**

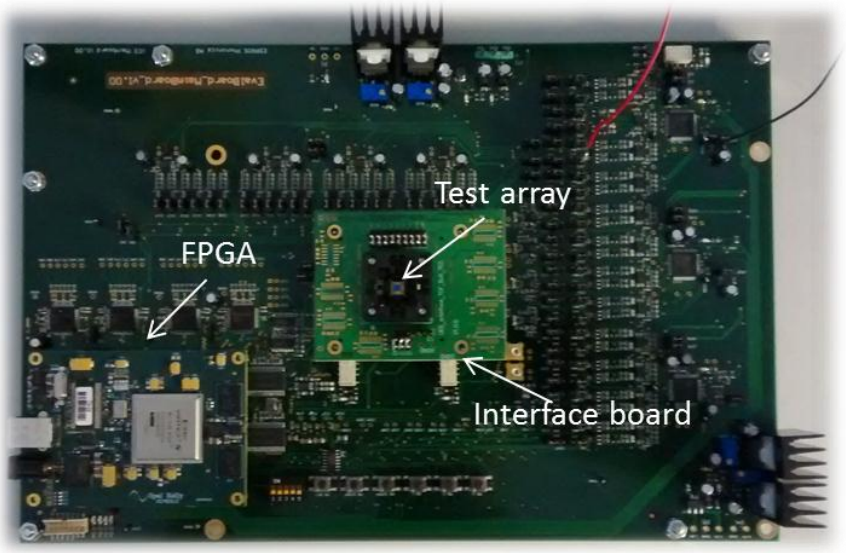

Figure 3: The UES main board with FPGA and interface mounted.

3. Characterisation

The aim of this work is to determine the electrical properties of EPC manufactured devices and test systems. The initial testing incorporates standard characterisation, such as conversion gain, read noise and full well capacity using a PTC. Dark current measurements were made at room temperature, without optical stimulus (i.e. the device is optically dark). The test procedures and results are summarised below.

3.1 Photon Transfer

The PTC was produced by uniformly illuminating the test device using a LED to approximate a flat field **[1]**. As the pixel array is small (8x8) a large number of images were captured at each integration time and averaged together to produce a single average frame.

These measurements allow a PTC, and hence a calibration value (conversion gain) to be produced for each individual pixel and eliminates the effects of an imperfect flat field (a result of using a LED) on fixed pattern noise. The conversion gain was calculated for each individual pixel and varies across the array between 24.7 µV/e^- and 28.8 µV/e^-, with an average conversion gain of ~27 µV/e^-.

The separate outputs present in each pixel of the test array result in different read noise and gain values for the same pixels, as shown in the un-calibrated PTC in Figure 4 where red and blue curves diverge.

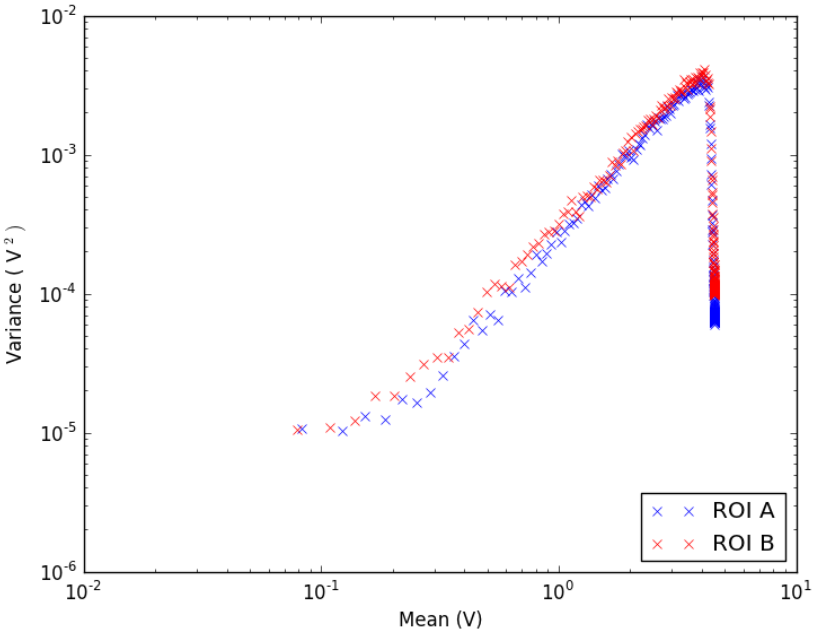

Figure 4: PTC produced as an average across the 8x8 test array. The different colours represent the two readout paths within each pixel, showing different values depending on readout A or B. Mean refers to the mean value of the flat field signal across the array, and Variance is the variance of the flat field signal across the array.

The pair of PTCs in Figure 4 was produced using a region of interest (ROI) within the 8x8 array. The ROI includes the core 7x7 pixels of the test array, the border pixels are excluded because they show significant fixed pattern noise during initial testing. Figure 4 shows the difference in gain characteristics caused by the separate outputs and also gives read noise of the sensor and UES mainboard where the gradient tends to zero at small signal.

3.2 Read Noise

The PTC shown in Figure 4 is produced by averaging across the test array within a ROI therefore the data includes fixed pattern and read noise components. Read noise is determined by the part of the curve which tends to a gradient of zero. The read noise value extracted from Figure 4 is 3.2mV RMS or ~117 e^- ENC. However this value is measured in the presence of a light source.

Further investigations have shown that the rms noise produced in the electronics alone (when no device is present), is between ~1.5 – 2 e^- ENC depending on the channel tested. Read noise measured again with the devices, and with no light source active inside the dark box can be measured as low as ~12 e^- ENC, this is significantly higher than the noise floor of the electronics alone. Figure 4 gives higher values for read noise because it was not possible to achieve a sufficiently small signal level with a LED illuminating the sensor, even with an integration time set to zero.

3.3 Full Well Capacity

The FWC was extracted from the photon transfer curve in Figure 4 where there was a drop in variance at ~4.5 V giving a value of ~200 ke^-. This presents an average value across the ROI. The FWC can also be determined for individual pixels and actually ranges from ~180 ke^- to ~220 ke^- due to the differing pixel designs within the test array.

3.4 Dark Current

Dark current is produced by interface states at the substrate-oxide boundary and impurities in the silicon substrate which reduce the energy required by electrons to cross the silicon band gap. The electrons produced as dark current are indistinguishable from signal electrons and therefore contribute to the noise characteristics of the sensor [1].

Dark current generation is measured when the device is optically dark (i.e. in a dark box and not exposed to any light source). The ambient temperature within the dark box is 40 °C measured using a digital mutli-meter, this is the temperature at which dark current measurements are made.

By capturing image frames over a range of integration times and calculating the mean signal across the array the signal per pixel was calculated. A plot of this value against the relevant integration time is presented in Figure 5. The gradient of the dark current trend line in Figure 5 gives a rate value of dark current generation of 3.6×10^6 $e^-.pix^{-1}.s^{-1}$ at 40 °C. This can be extrapolated to ~80 nA/cm² at 20 °C as there is an exponential relationship between temperature and dark current.

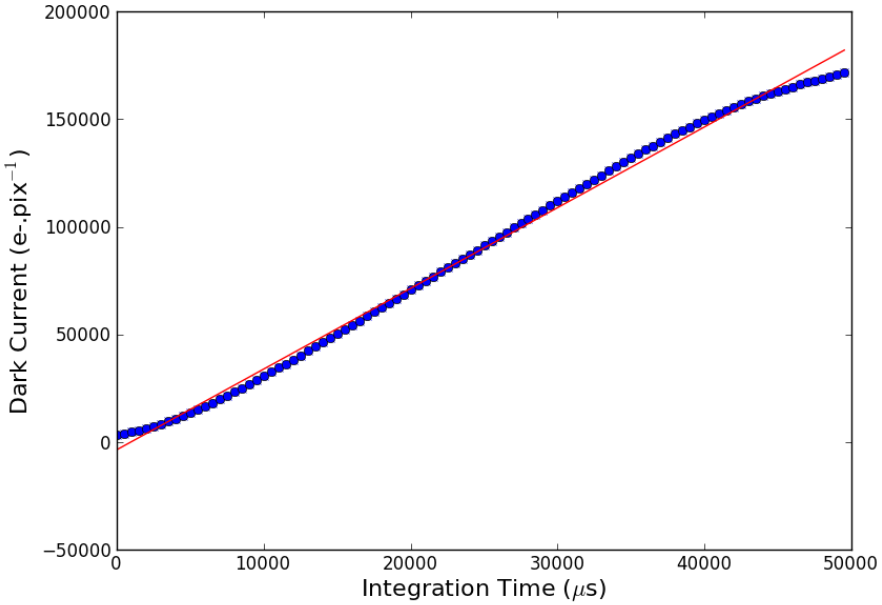

Figure 5: The dark current generation per pixel as an average across the array, where Integration Time is the total time which the modulation gate is actively transferring charge to the storage gate. The dark current generation rate is calculated from the gradient of this data (given by the linear fit represented by the red line), giving 3.6×10^6 $e^-.pix^{-1}.s^{-1}$ at 40 °C. The linear fit also demonstrates that the dark current distribution varies around the expected linear trend, which can be attributed to a variation in temperature during measurement.

The dark current generation rate, calculated from Figure 5, is an average across the entire 8x8 array, however differences in dark current are expected due to the changes in pixel design across the array. Dark current is also calculated on a pixel by pixel basis and plotted as a heat map in Figure 6 to represent the dark current generation rate in each individual pixel. Figure 6 uses the linear fit method introduced in Figure 5, and also uses each pixels individual conversion gain value. Figure 6 shows that the dark current varies across the array, and is significantly larger in one half of the array than in the other. The changes in dark current generation can be attributed to the difference in the size of the storage gates in the different pixel designs.

Figure 6 is an 8x16 array (rather than 8x8) because an image is produced from both storage/ readout paths present in each pixel. The data produced from storage gate A is the left 8x8 section and the data from storage gate B is the right 8x8 section.

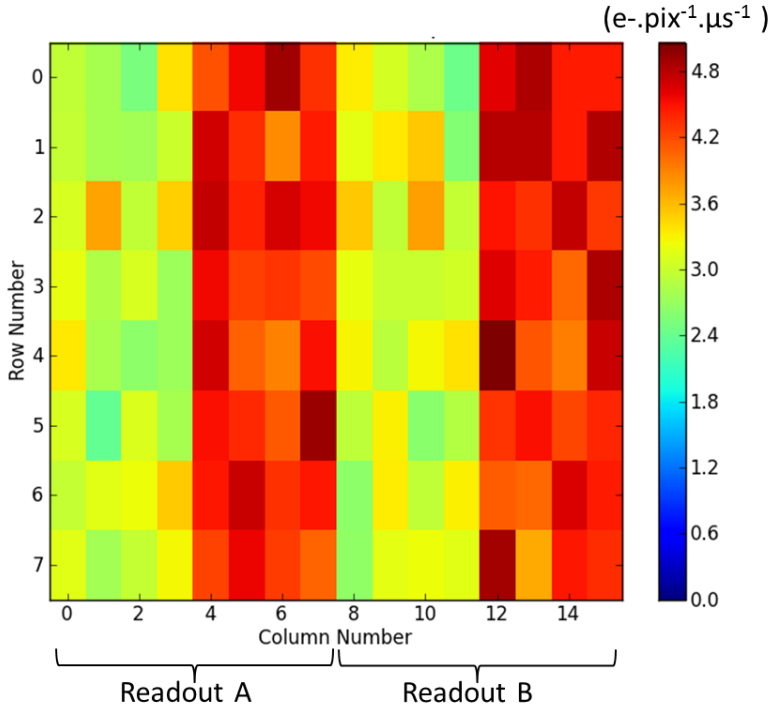

Figure 6: Heat map of the dark current calculated for each pixel, in units of $e^{-}.pix^{-1}.\mu s^{-1}$, showing the change between the two halves of the array which feature different pixels. The left 8x8 section represents signal from readout path A, while the right 8x8 section represents signal from readout path B.

Dark current generation in the first section of the array (pixels 0 – 3 on the x-axis) gives an average value of $3x10^{6}$ $e^{-}.pix^{-1}.s^{-1}$ at 40 °C, while dark current generation in the second half of the array (pixels 4 – 7 on the x-axis) gives an average value of 4.5 $x10^{6}$ $e^{-}.pix^{-1}.s^{-1}$ at 40 °C. The difference in dark current generation rate can be associated with the change in storage gate sizes, with higher dark current in those pixels with larger storage gates. Work is ongoing to produce test equipment to enable cooling which should suppress dark current.

4. Depletion Depth

The devices tested for this study are back illuminated, and as such it is important to check that they are fully depleted under normal operating conditions. It is possible to determine the depletion depth by projecting a spot onto the test device [4] [5]. By changing bias voltages which control thedepletion depth, such as the backside bias voltage, it should be possible to detect changes to the peak value of the spot due to charge diffusion. Both the backside bias voltage (Vbs) and the drift gate voltage (Vdg) are expected to impact significantly on depletion depth, so both were tested.

Figure 7 shows the spot projected onto the test device. A plot of the peak spot signal versus integration time, also in Figure 7, demonstrates the linearity and repeatability of the spot characteristics. The peak amplitude of the spot signal in Figure 7 is in pixels (4, 1) and (12, 1) corresponding to readout paths A and B.

The projected spot should ideally be smaller than one pixel. The spot in Figure 7 is limited to approximately four pixels, however the repeatability of the spot characteristics is good and the signal in the peak pixel is reasonably linear as integration time increases. This enables the analysis of the peak spot signal as bias levels are adjusted.

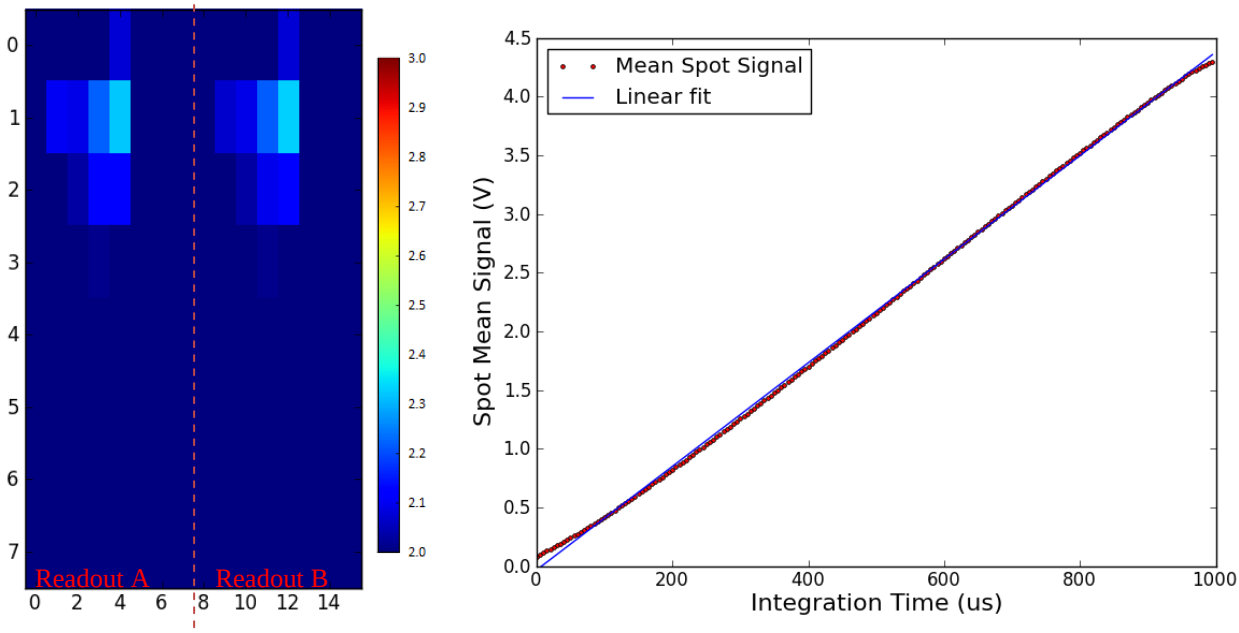

Figure 7: Spot projection, left, showing the spot produced for each readout path (A and B). The peak spot location is (4, 1) and (12, 1). The graph on the right shows the peak amplitude of the spot averaged over ~100 frames (hence spot mean signal), plotted against integration time to demonstrate the spot linearity over the full integration range and its repeatability.

Figure 8 shows the how the peak value of the spot signal changes while adjusting the backside bias voltage (Vbs) and keeping the integration time constant. An increase in peak value is observed as Vdg increases, plateauing around the recommended Vbs level of -3V. The peak signal value remains constant when the device is operated beyond the recommended Vbs value, implying that the depletion depth has extended to its maximum and the device is fully depleted. As the voltage becomes less negative the depletion depth will reduce, causing the peak signal value to drop.

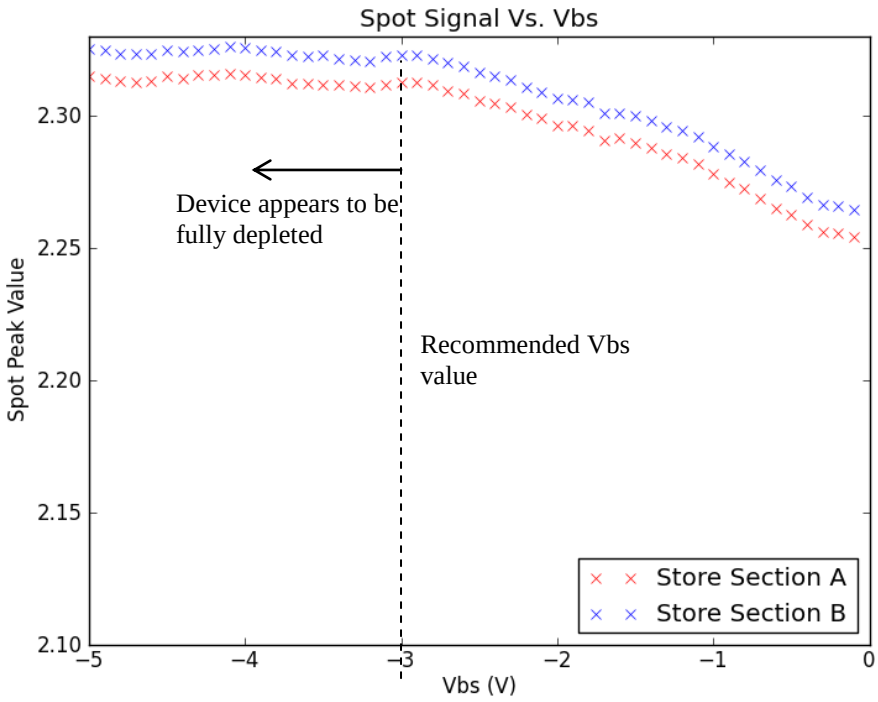

Figure 8: Change in spot peak signal caused by altering the backside bias voltage in the test devices, while keeping the integration time constant. Red and blue colours represent the values measured through each of the readout paths (A and B). The dotted line indicates the manufacturers recommended voltage setting.

Figure 9 shows how the peak value of the spot signal changes as the voltages applied to the drift gates change, while keeping all other parameters, including integration time, at a constant value. The drift gate voltage settings are monotonically increasing from Vdg3 (lowest voltage), to Vdg1 (maximum voltage), as described in Section 2. Figure 9 scans a value of Vdg_max on the x-axis, which refers to the voltage applied to Vdg1, with the other drift gates monotonically decreasing in voltage value from this maximum. The peak spot signal amplitude increases as the Vdg bias increases, until it plateaus around the recommended bias value of 4V. The amplitude of the signal through readout path A increases at 5V, this is not thought to be related to a change in the depletion region as this is isolated only to one readout path. The trends of readout paths A and B were expected to closely match, as in Figure 8.

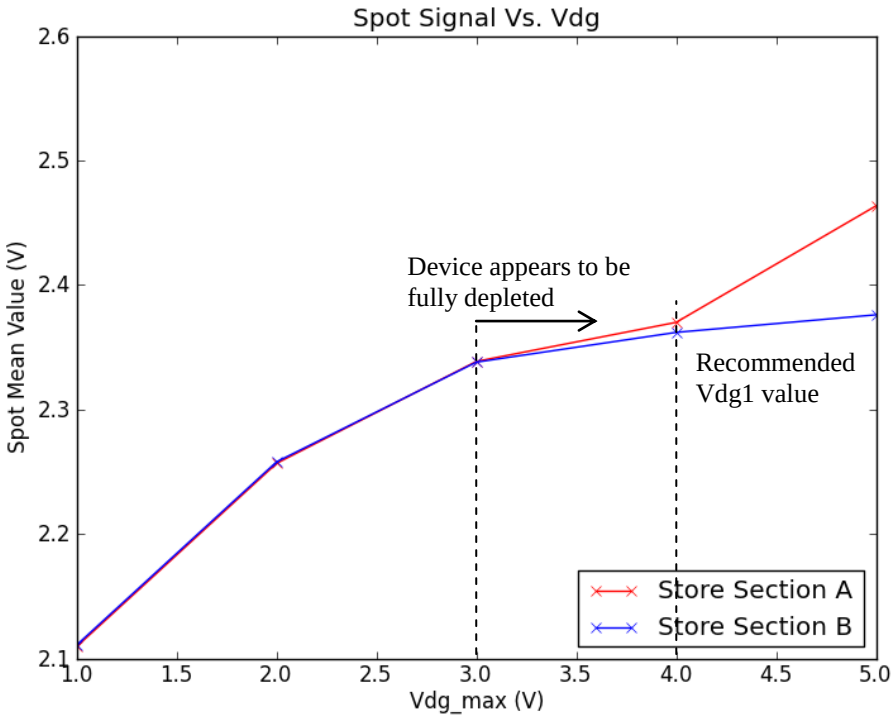

Figure 9: Change in spot peak signal amplitude caused by altering the drift gate bias voltages in the test devices, while holding all other parameters at constant values. Red and blue curves represent each of the available readout paths (A and B)

The backside bias has a much smaller influence over the peak spot amplitude than is observed in the Vdg tests. The plateaus observed in both the backside bias and drift gate measurements indicate that the device has become fully depleted at the recommended bias levels.

5. Conclusions and Outlook

The aims of this work were to characterise the electrical properties of the EPC devices and camera electronics. The work involved characterising the conversion gain, FWC, read noise and dark current generation rate. The test device worked well; even though the array size is relatively small, a reliable PTC can be produced both as an array average and on a pixel- by-pixel basis. The device shows some variation in FWC and dark current generation across the array, presumably caused by the differing pixel designs present in the array.

Further work involved determining if the device was fully depleted during normal operation. This was achieved using a spot projection and adjusting the bias levels which control the depletion region, while keeping other operating parameters constant. As the depletion depth changes with the applied bias, the amplitude of the signal level of the projected spot changes. This experiment indicated that the device is fully depleted (to 50 µm) during normal operation. A fully depleted structure is important for good quantum efficiency of back illuminated devices.

These initial measurements help to improve our knowledge of the EPC manufacturing process and test equipment which will be used to further evaluate these and future devices. Characterisation using a x-ray source is planned once a test bench has been commissioned for cooling the device to suppress dark current.

Acknowledgments

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